Heiko Joerg **Schick**

Chief Architect | Advanced Computing

linkedin.com/in/heikojoergschick +49-151-54682218 heiko.schick@huawei.com info@schihei.de
http://www.schihei.de Munich, Bavaria, Germany German Citizen

I am Chief Architect for Huawei Technologies, a leading global provider of information and communication technology. My expertise in artificial intelligence, novel computer architectures, and heterogeneous computing has helped Huawei become a global leader in developing technologies that will shape the modern world for years to come. Aside from my contributions to propelling Huawei to become one of the most innovative technology companies in the world, I have also helped foster an environment of trust, diversity, and open-mindedness.

Professional experience

Present – January 2019

Chief Architect | HiSilicon Turing Department, Huawei Technologies, Germany

- Enabling Arm for HPC / Arm+AI ecosystem with cooperation partners to foster the use of HiSilicon solutions, gathering requirements for next generation server systems
- Support HQ HiSilicon R&D team in designing efficient SoC architectures for advanced computing and autonomous driving
- Represent Huawei in standardisation and industry activities such as EU-level strategy shaping activities like the European Technology Platform for HPC (ETP4HPC)
- Drive technical academia engagement programs and cooperation projects
- Hiring for HiSilicon team for advanced computing – this includes screening candidate profiles, supporting interviews, refinement of job descriptions and coordination with recruiters

During my time in this position, I have successfully matched candidates against job roles and classified suitability. I have also orchestrated the deployment of Huawei's server and AI hardware with many partners, who are active in computer vision, machine learning, scientific computing or supercomputing.

Artificial Intelligence | Supercomputing | HPC | ARM

December 2018 – January 2015

Chief Architect | Central Hardware Department, Huawei Technologies, Germany

- Led and hired a team of >7 experts with a focus on computation (micro-architecture), interconnect and memory technologies
- Successfully orchestrated and organised a project charter for an Arm-based advanced computing prototype, including the definition of project scope, key technologies and milestones
- Defined architectural elements and improvements for Arm-based computing systems in the areas of computation, memory system, storage, switching and interconnect
- Identified and researched on new key technologies contributed to the Huawei's system strategies
- Facilitated the architectural concept for in-memory processing technologies for the use in Arm-based systems
- Collaborated with three significant research and data centres in Europe to evaluate Arm-based systems and make experimental hardware codesign
- Established partnerships for Horizon 2020 projects on advanced computing
- Principal representative to the Cache Coherent Interconnect for Accelerators (CCIX) standard, implemented in HiSilicon Kunpeng 920 SoC
- Defined high-impact libraries and performance tools for the Arm architecture, generated requirements and executed performance optimisation
- Contributed to the incubation of a team which is focusing on autonomous driving

ARM | Computer Architecture | HPC | In-Memory Processing | CCIX | ETP4HPC | Research Collaborations

December 2014 – January 2014

Senior Engineer | Systems Optimisations Competency Center, IBM Research & Development, Germany

- Led the technical and performance team for the SAP HANA in-memory, column-oriented, relational database management system on the IBM POWER architecture
- Ensured that the performance result is on par with competitive hardware configurations
- Provided support to achieve performance objective by leading POWER specific code development and executing performance evaluation
- Analysed utilisation of hardware resources (memory bandwidth, threads, cores and sockets) during intensive scaling tests
- Defined the scale-out and scale-up system architecture and execute corresponding performance measurements
- Investigated hot functions on micro-architecture level
- Improved vector code coverage in SAP HANA by 6%, leading to 15% more performance

SAP HANA | IBM System p | POWER Architecture | SAP-H | Springer | BW-EML

December 2013 – July 2011

Senior Engineer | Blue Gene Active Storage, IBM Research & Development, Germany

- Led the technical engineering team of >8 people, which was responsible for the development and delivery of the Blue Gene Active Storage (BGAS) architecture
- Successfully contributed to the BGAS architecture to achieve a balanced integration of solid-state storage, computation, and cost-scaleable network
- Leveraged Blue Gene/Q as a vehicle for rapid prototyping for active storage concepts
- Executed proofs-of-concept on computing-in-storage for applications in neuroscience and middleware software packages including GPFS and DB2
- Responsible for the architecture and development of software packages (including peripheral image, device driver, FPGA image and middleware frameworks) for a hybrid scalable solid-state storage device, which targeted research explorations
- Decomposed acceleration function for industrial and scientific application scenarios
- Responsible for the development of a software-based RDMA network interface controller
- Coordinated research engagements with three customers in Germany, Switzerland and the United Kingdom
- Mentored bachelor and master students

Blue Gene/Q | Active Storage | BGAS | Computing-in-storage | GPFS | DB2 | Solid-state-storage

June 2011 – April 2009

Senior Engineer | Blue Gene/Q, IBM Research & Development, Germany

- Led a global PCI Express verification and performance team for the Blue Gene/Q ASIC to complete ahead of schedule and within the expected performance promises
- Led and executed the hardware bring-up of the PCI Express core of the Blue Gene/Q ASIC
- Create the verification and performance plan and regularly reported status to executive management and customers
- Developed proxy applications to simulate parallel file-system traffic tunnelled via InfiniBand over PCI Express
- Created a hardware simulation environment to imitate the operation of the Blue Gene/Q ASIC in combination with PCI Express attached devices (including physical, link and transport layer)
- Implemented an automatic regression framework for I/O traffic on ASICs

Blue Gene/Q | PCI Express | InfiniBand | Parallel Filesystems | ASIC | Simulation

March 2009 – January 2008

Resident Engineer | Open Systems Development, IBM Research & Development, Germany

- Led the bring-up of the QPACE project and coordinated >15 developers from industrial and academic partners
- Responsible for the architecture and the development of the firmware for the compute node of the QPACE project
- Developed the bring-up plan for the QPACE project

Supercomputer | Prototype | Research Project | Cell/B.E

December 2007 – September 2006

Resident Engineer | Open Systems Development, IBM Research & Development, Germany

- Contributed to the firmware development of blade servers using the PowerPC 970 and Cell/B.E. processor
- Responsible for the PCI Express device discovery algorithm
- Ensured the hardware bring-up, compatibility and performance of PCI Express-based InfiniBand adapters
- Accountable for the PCI Express compliance testing with a focus on the physical layer, configuration space, link & transport layer and platform configuration
- Led the AbiCell and NICOLL project

Linux | Firmware | PCI Express | InfiniBand | Cell/B.E. | PowerPC 970

August 2006 – September 2004

Staff Engineer | I/O Firmware Development, IBM Research & Development, Germany

- Developed the Linux kernel framework and interrupt processing routines for the IBM System p InfiniBand and Ethernet device driver
- Ensured compatibility and performance towards upper-level protocols such as the Message Passing Interface (MPI) standard, Socket Direct Protocol (SDP) and communications using TCP/IP over InfiniBand
- Coordinated the open-source and release process with the Linux kernel development community and Linux distributors
- Led the technical bring-up and development of a parallel cluster based on the PowerPC 970 processors and ultra-low latency InfiniBand network components
- Contributed to software optimisations and performance tests to make QPACE to the most energy-efficient supercomputers of June 2010

Linux | Linux Kernel | Network | InfiniBand | Ethernet | IBM System p

August 2004 – Mai 2004 | **Diploma Thesis | Processor Firmware Development, IBM Research & Development, Germany**

Concept, Design and Implementation of a Slimline Boot Firmware for Linux on Power Architecture.

- Specified, implemented and demonstrated the technology on how binary program code can be packaged within the firmware and executed later, by the operating system, with the usage of a small-footprint virtual machine.

Research Concept | Firmware | Operating System | Virtual Machine

April 2004 – January 2003 | **Internship | Processor Firmware Development, IBM Research & Development, Germany**

- Implemented a Linux program to trace program execution machine instructions
- Analysed how machine instructions will execute in several processor pipelines of IBM mainframes

Linux | Assembler | C | Processor Pipelines | IBM System z

October 2002 – July 2002 | **Student Employee | Linux on System z Evaluation, IBM Research & Development, Germany**

- Developed and executed a test plan for running >100 Linux instances in a virtual machine environment on IBM mainframes
- Verified performance advantages of sharing hardware and software resources in overcommitment scenarios and during high-speed network communications

Linux | Virtual Machines | IBM System z | z/VM

February 2002 – August 2001 | **Internship | Linux on System z Evaluation, IBM Research & Development, Germany**

- Developed and executed a test plan for a cryptographic Linux device driver for IBM mainframes
- Verified task offloading to installed cryptographic co-processors and acceleration devices
- Developed an automatic test framework the execution of all verification tasks

Linux | Linux Kernel | Device Driver | Perl | IBM System z

Education

August 2004 – October 2000 | **Communication and Software Engineering, Albstadt-Sigmaringen University, Germany**

Final Grade: 1.2

Operating Systems | Computer Architecture | Communication Networks | Software Architecture

Outreach and volunteering

2019 **CODES@OEHI Hackathon**, Two-day hands-on workshop for current or prospective users of Arm-based HPC system to port their applications to such system or to further optimise already ported applications.

March 2010 – February 2010 | **Technical Consultant, IBM Research & Development, Philippines**

Volunteer Experience for IBM Corporate Service Corps, Disaster and Humanitarian Relief

- Consulted the National Institute of Geological Sciences (NIGS) on how to create interactive real-time flood maps of Metro Manila
- Consulted the design and developed a reference system of a flood prediction system
- The project received for its outstanding initiative in corporate social responsibility by an Excellence Award of the Asian CSR Awards

Flood Simulation | Flood Prediction | Real-time Flood Maps | HPC

Skills

Programming Languages	**C**, **C++**, Java, Forth, Javascript, CSS, XML, XSLT, Ruby, Python, Perl
Frameworks	MPI, Cuda, Hadoop, PROOF | ROOT, Linux Device Driver
Databases	MySQL, SQLite, SAP HANA, MySQL, Oracle Database
Development Tools	Make, Configure, GNU toolchain, Ant, SVN, git
Middleware	GPFS, Open Fabrics RDMA Stacks
Operating Systems	Mac OS X, Windows Server, Windows 7, Linux Redhat, Linux CentOS
Others	UML

Publications

2013 El Sayed, S., Graf, S., Hennecke, M., Pleiter, D., Schwarz, G., Schick, H., & Stephan, M. **Using GPFS to manage NVRAM-based storage cache**. Lecture Notes in Computer Science (Including Subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 7905 LNCS, 435–446.
https://doi.org/10.1007/978-3-642-38750-0_33

2010 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **QPACE: Power-efficient parallel architecture based on IBM PowerXCell 8i**. Computer Science - Research and Development, 25(3–4), 149–154.
https://doi.org/10.1007/s00450-010-0122-4

2010 Strunk, J., Hiltscher, J., Rehm, W., & Schick, H. **Communication architectures for run-time reconfigurable modules in a 2-D mesh on FPGAs**. Proceedings - 2010 International Conference on Reconfigurable Computing and FPGAs, ReConFig 2010, 49–54.
https://doi.org/10.1109/ReConFig.2010.33

2009 Strunk, J., Heinig, A., Volkmer, T., Rehm, W., & Schick, H. J. **Run-Time Reconfiguration for HyperTransport Coupled FPGAs using ACCFS**. First International Workshop on HyperTransport Research and Applications.

2009 Strunk, J., Volkmer, T., Stephan, K., Rehm, W., & Schickz, H. **Impact of run-time reconfiguration on design and speed - A case study based on a grid of run-time reconfigurable modules inside a FPGA**. IPDPS 2009 - Proceedings of the 2009 IEEE International Parallel and Distributed Processing Symposium.
https://doi.org/10.1109/IPDPS.2009.5161221

2009 Schick, H. J. **directCell: The Cell/B.E. as a Tightly Coupled Accelerator**. International Supercomputing Conference.

2009 Penner, H., Bacher, U., Kunigk, J., Rund, C., & Schick, H. J. **DirectCell: Hybrid systems with tightly coupled accelerators**. IBM Journal of Research and Development, 53(5).
https://doi.org/10.1147/JRD.2009.5429068

2009 Strunk, J., Volkmer, T., Rehm, W., & Schick, H. **Design and performance of a grid of asynchronously clocked run-time reconfigurable modules on a FPGA**. ReConFig'09 - 2009 International Conference on ReConFigurable Computing and FPGAs, 392–397.
https://doi.org/10.1109/ReConFig.2009.24

2009 Schick, H. J. Communication Networks Attached to the IBM PowerXCell 8i I/O Fabrics. Workshop for Network Specification and Software Data Structures for the eQPACE Architecture.

2009 Schick, H. J. **Cell/B.E. tightly coupled via PCI Express. Workshop about Future Activities on High Performance Computing.**

2009 Strunk, J., Volkmer, T., Rehm, W., & Schick, H. **An on chip network inside a FPGA for run-time reconfigurable low latency grid communication**. 12th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, DSD 2009, 539–546.
https://doi.org/10.1109/DSD.2009.133

2009 Heinig, A., Strunk, J., Rehm, W., & Schick, H. **ACCFS - operating system integration of computational accelerators using a VFS approach**. Lecture Notes in Computer Science (Including Subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 5453, 374–379.
https://doi.org/10.1007/978-3-642-00641-8$_4$4

2009 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **QPACE – a QCD parallel computer based on Cell processors**. Proceedings of Science.
http://arxiv.org/abs/0911.2174

2008 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **Status of the QPACE Project**. XXVI International Symposium on Lattice Field Theory.
http://arxiv.org/abs/0810.1559

2008 Schick, H. J., Fischer, U., Pleiter, D., Wettig, T., & Lippert, T. **QPACE: QCD Parallel Computing on Cell/BE**. International Conference for High Performance Computing, Networking, Storage and Analysis.
http://sc08.supercomputing.org/scyourway/conference/view/post129.html

2008 Heinig, A., Strunk, J., Oertel, R., Rehm, W., & Schick, H. J. **Generalizing the SPUFS concept - A Case Study towards a Common Accelerator Interface**. Many-Core and Reconfigurable Supercomputing Conference.

2008 Heinig, A., Rehm, W., & Schick, H. J. **ACCFS (Accelerator File System) - A Case Study Towards a Generalized Accelerator Interface**. International Supercomputing Conference.

2008 Goldrian, G., Huth, T., Krill, B., Lauritsen, J., Schick, H., Ouda, I., … Fodor, Z. **QPACE: Quantum Chromodynamics Parallel Computing on the Cell Broadband Engine**. Computing in Science and Engineering.

2008 Schick, H. J., Penner, H., Hering, H., & Wohlmuth, O. **Cell/B.E. Accelerator Concept**. IBM Technical Leadership Exchange Conference.

2007 Schick, H. J., Penner, H., & Wohlmuth, O. **Slimline Open Firmware**. Power Architecture Developer Conference.

2007 Detert, U., Thomasch, A., Eicker, N., & Broughton, J. **JULI Project-Final Report**.

2007 Strunk, J., Heinig, A., Rehm, W., & Schick, H. J. **Heterogeneous Multiprocessing - On a Tightly Coupled Opteron Cell Evaluation Platform**. IBM CAS Software and Systems Engineering Symposium.

2007 Schneider, T., Wunderlich, S., Rehm, W., Hoefler, T., & Schick, H. J. **Code Optimization for Cell/B.E. - Opportunities for ABINIT - A Software Package for Physicist**. IBM CAS Software and Systems Engineering Symposium.
2007 Penner, H., Schick, H. J., Wohlmuth, O., & Hering, H. **CELL/B.E. Accelerator Concept.** IBM Early Career Conference.
2007 Schick, H. J., & Kunigk, J. **An Open Firmware**. IBM Academy of Technology Conference.
2005 Wohlmuth, O., Penner, H., Schick, H. J., Boessenkool, S., & Koch, S. **Slimline Open Firmware**. Power.Org Event in Barcelona.
2005 Schick, H. J. **Concept, Design and Implementation of a Slimline Boot Firmware for Linux on Power Architecture**. Diploma Thesis.

Lectures and talks

2020 **Huawei empowers healthcare industry with artificial intelligence technologies**, Emerging Technologies in Medicine
2019 **The Smarter Car for Autonomous Driving**, GSA European Executive Forum
2019 **Challenges of Autonomous Driving**, Association of German Engineers.
2018 **From edge computing to in-car computing**, Elektrobit Innovation Day.
2017 **Panel Discussion: Super-Computing versus Quantum Computing**, golemconference - Dawn of the Quantum Era.
2016 **Future of Hardware Architectures – Do we need new System Concepts for Artificial Intelligence?**, TNG Big Techday.
2011 **Petascale Analytics**, STRONGnet 2011 at the European Centre for Theoretical Studies in Nuclear Physics.
2011 **High Performance Computing**, Guest Colloquium for the Research Training Group LORENTZ FORCE, Lorentz Force Velocimetry and Lorentz Force Eddy Current Testing at the University of Ilmenau.
2011 **IBM Corporate Service Corps: Helping Create Interactive Flood Maps**, Association of German Engineers.
2011 **Experiences in Application Specific Supercomputer Design: Reasons, Challenges and Lessons Learned**, PRACE/LinkSCEEM-2 2011 Winter School in Nicosia.
2009 **Research Project QPACE – QCD Parallel Computing on the Cell Broadband Engine**, Association of German Engineers.
2005 **High Performance Computing: Blue Gene/L**, Association of German Engineers.
2004 **The IBM Cell Processor - Computing of tomorrow or yesterday?**, Association of German Engineers

Patents

2010 PCI Express multiplier device, computer system, method for operating PCI Express devices in a computer system, computer program product, and data processing program for operating PCI Express devices in a computer system.
2008 Apparatus for analyzing communication between a blade server and its expansion units or daughter cards.

Honors and awards

2019 Huawei Science and Technology Diplomacy Award
2019 Huawei Handshake Award
2015 Huawei Rising Star Award
2010 Excellence Award of the Asian CSR Awards
2010 IBM First Patent Application Invention Achievement Award
2009 IBM Equity Award
2006 IBM Bravo! Award
2005 IBM Author Recognition Award
2004 Award of the Philipp-Matthaeus-Hahn Donation

Languages skills

German ●●●●●
English ●●●●●
French ●○○○○

Strengths

- Immerse in different cultures
- Understand the people around me
- Promote an environment of trust, diversity, and open-mindedness

Projects

Blue Gene Active Storage 2011 - 2013

https://www.slideshare.net/schihei/blue-gene-active-storage
Blue Gene Active Storage (BGAS) is a model for storage embedded parallel processing as that addresses exascale data intensive challenges. BGAS is aimed at emerging scalable system-on-a-chip, storage class memory architectures and is realized in prototype form on current parallel systems. BGAS can be used to transparently accelerate host workloads by close integration at the middleware data/storage boundary or directly by data intensive applications.

Tag

Exascale Innovation Center (EIC) 2011 - 2013

https://www.fz-juelich.de/ias/jsc/EN/Research/HPCTechnology/ExaScaleLabs/EIC/_node.html
The Exascale Innovation Center (EIC) is a joint research collaboration between the Juelich Supercomputing Centre (JSC), Forschungszentrum Juelich and IBM. It will focus on addressing the tremendous challenge, and opportunity, that exascale computing allows. Unprecedented challenges in energy discovery, energy optimization and climate prediction all require supercomputing resources. Success at the exascale can only be achieved through a comprehensive program that includes all aspects from core technology through applications and algorithms.

Tag

Blue Gene/Q 2009 - 2011

https://en.wikipedia.org/wiki/IBM_Blue_GeneBlue_Gene/Q
Blue Gene is an IBM Research project to explore the frontiers in supercomputing, in computer architecture, in the software required to program and control massively parallel systems and in the use of computation to advance the understanding of biological processes, hydrodynamics, quantum chemistry, quantum chromodynamics, molecular dynamics, climate modelling and financial modelling.

Supercomputer | HPC | PCI Express

QPACE 2008 - 2009

https://en.wikipedia.org/wiki/QPACE
QPACE pursued the development of a massive parallel, scalable supercomputer for applications in lattice quantum chromodynamics (QCD). The machine structure is a three-dimensional torus of identical processing nodes, based on the IBM PowerXCell 8i processor. These nodes are tightly coupled by an FPGA-based, application-optimized network processor attached to the IBM PowerXCell 8i processor. The development of QPACE was a common effort of several academic institutions together with the IBM Research and Development Lab in Boblingen, Germany. The academic partners included the Universities of Regensburg and Wuppertal as well as the research labs DESY and Juelich and the Universities of Ferrara and Milano.

Supercomputer | HPC | Cell/B.E.

AbiCell 2006 - 2007

https://www.scribd.com/document/23345235/Code-optimization-for-Cell-B-E...
The goal of this project was to study the performance potential of InfiniBand connected Cell clusters by implementing selected parallel compute kernels of Abinit, a widely-used open source code for ab initio electronic structure calculations.

Parallelization | HPC | Cell/B.E.

NICOLL 2006 - 2007

https://www.scribd.com/doc/23362882/Heterogeneous-Multiprocessing-On-a-tightly-coupled...
The objective of this project was to develop a prototype solution for an interface architecture that fits best the needs of the Cell/B.E. processor HW-SW infrastructure in hybrid systems. When necessary, techniques of device virtualization were applied. The focus is on interfacing InfiniBand as an example solution for a high-speed cluster interconnects technology. With respect to collective communication operations the focus was on the Message Passing Interface (MPI).

Hybrid System | Computer Architecture | Cell/B.E. | Networking | InfiniBand

eHCA InfiniBand Adapter 2004 - 2006

https://git.kernel.org/pub/scm/linux/kernel/git/stable/linux.git/tree/drivers/infiniband/hw/ehca?h=v3.16.81
The adapter is used in high-performance computing (HPC) clusters. The device driver was developed for Linux on PPC64 and is compatible with the unified Open Fabrics Alliance open-source software stack for InfiniBand which is one of the major RDMA technologies. To leverage the eHCA InfiniBand adapter an application can call directly IB verbs or uses upper-level protocols like the Message Passing Interface (MPI), TCP/IP over InfiniBand (IPoIB) or Socket Direct Protocol (SDP). The device driver is included in Linux kernel since 2.6.19.

Linux | Linux Kernel | Networking | InfiniBand

eHEA Ethernet Adapter 2004 - 2006

https://git.kernel.org/pub/scm/linux/kernel/git/stable/linux.git/tree/drivers/net/ethernet/ibm/ehea?h=v3.16.81
The network adapter is used in IBM POWER6 based systems. The device driver supports the network main functionality including TCP segmentation offload (TSO), broadcast, multicast, VLAN and ethtool. It is included in Linux kernel since 2.6.19.

Linux | Linux Kernel | Networking | Ethernet